

SWITCHING POWER SUPPLY UNIT AND CONTROLLER IC THEREOF

Background of the Invention

Field of the Invention

The invention relates to a switching power supply
5 unit which switches input voltage to produce output voltage
that is different from the input voltage, and to a
controller IC thereof.

Description of the Related Art

10 In a portable cellular phone, a digital camera, a
PDA, and a personal computer, a higher DC voltage is often
required to be produced from a low power supply voltage
such as a battery cell. In such a case, the higher DC
voltage might be produced from a switching power supply
15 unit, however, in many cases, it might be difficult for an
actual apparatus to perform all the control operations,
including a PWM control operation, at a low power supply
voltage. For this reason, a conventional switching power
supply unit is provided with a low-voltage operating block
20 capable of operating at a low voltage within the range from
1.0 to 1.5 volts or thereabouts such as disclosed in JP-A-
8-186980. In said reference, disclosed is the circuit
configuration such that ,at start up timing, a battery
voltage is first boosted up to a voltage at which another

regular operating block for performing PWM control or the like can be operated, by means of the low-voltage operating block. Subsequently, to the operation is shifted to the regular PWM control operation.

5 Fig. 3 is a view showing the configuration of a switching power supply unit 200 in which such a conventional switching power supply unit has been partially modified in accordance with actual use, thereby producing a higher DC voltage from a low power supply voltage. Fig. 4
10 is a view schematically showing a characteristic of the start-up of the switching power supply unit 200 shown in Fig. 3.

 In Fig. 3, a battery BAT, such as the one including two nickel hydrogen battery cells, is serving as a DC power
15 supply use, whose battery voltage V_{bat} of the battery is about 1.5 volts. The voltage V_{bat} is connected to the earth by way of an inductor L_o and a switching transistor Q_o serving as an NPN transistor. The switching transistor Q_o is switched between on and off in response to a
20 switching control signal S_{out} . A collector voltage of the switching transistor Q_o is rectified and smoothed by a rectifier diode D_o and a smoothing capacitor C_o , whereby an output voltage V_o is output (e.g., 5.0 volts is output at the time of a stationary state).

25 The switching control signal S_{out} provided to the

switching transistor Q_0 is produced and output by a controller IC 20. A commonly-used voltage control method is to feed back the output voltage V_o , compare the output voltage V_o with a reference voltage to produce an error
5 signal which is compared with a triangular wave signal so as to produce a pulse width modulation (PWM) signal, and perform a switching-control to the switching transistor Q_0 according to the pulse width modulation signal.

However, an actual apparatus often encounters
10 difficulty in performing all control operations such as PWM control operation at a low voltage on the order of 1.5 volts or thereabouts. Therefore, the switching power supply unit shown in Fig. 3 has a low-voltage operating block LVB which is capable of operating at a low voltage
15 (e.g., 1.5 volts). At start-up, the low-voltage operating block LVB boosts the battery voltage V_{bat} to a voltage (e.g., 2.5 volts) at which another ordinary high-voltage operating block HVB for performing PWM control or the like can operate. Subsequently, this system shifts operation to
20 an ordinary PWM control operation.

The configuration of the controller IC 20 will be further described. The battery voltage V_{bat} is input to a battery voltage terminal P_{bat} of the controller IC 20, which is provided to individual circuits operated at a low
25 voltage. Further, the output voltage V_o is input directly

to an output voltage terminal Pvo of the controller IC 20. The output voltage Vo serves as a comparison input for a comparator CP0, and also fed to the individual circuits which require a high voltage. Further, the feedback
5 voltage Vfb obtained by the output voltage Vo being divided by potential-divider resistors R1, R2 is input to a feedback voltage terminal Pfb.

The high-voltage operating block HVB that operates under normal conditions has an error amplifier Eamp which
10 outputs an error output signal E0 between the feedback voltage Vfb and a second reference voltage Vref2 which is fed back from an error output terminal Peo to the feedback voltage terminal Pfb by way of a feedback capacitor C1 and a resistor R3; a triangular wave signal oscillator OSC2; a
15 PWM comparator CP2 which receives a triangular wave signal CT output from the oscillator OSC2, an error output signal E0, and a soft start voltage (hereinafter, "SS voltage") Vss serving as a dead time control (DTC) voltage; and a second driver DR2 which amplifies an output of the PWM
20 comparator CP2 which is output as the control signal Sout from a second control signal output terminal Pout2.

The PWM comparator CP2 compares the triangular wave signal CT with the error output signal E0 or the SS voltage Vss, whichever signal is smaller. The second driver DR2
25 operates when an operating command signal (low level

voltage in this case) is given to. The high-voltage operating block HVB cannot be operated sufficiently when the output voltage V_o is equal to or slightly higher than the battery voltage V_{bat} . Consequently, the second
5 reference voltage V_{ref2} or the SS voltage V_{ss} , whichever signal is smaller, serves as a reference voltage for controlling the high-voltage operating block HVB.

The low-voltage operating block LVB, operating at the start-up timing, has an oscillator OSC1 which starts
10 oscillating upon receipt of the supplied battery voltage V_{bat} , to thus produce a rectangular wave pulse; and a first driver DR1 which amplifies a pulse produced by the oscillator OSC1 to be output as the control signal S_{out} from a first control signal output terminal Pout1. The
15 first driver DR1 operates when an operating command signal (high level voltage in this case) is given to. The low-voltage operating block LVB operates sufficiently at the battery voltage V_{bat} regardless of the output voltage V_o .

The comparator CP0 compares the output voltage V_o
20 with the first reference voltage V_{ref1} , thereby produces a high-level or low-level output as a comparison result. The first reference voltage V_{ref1} is set to a voltage at which individual circuits of the high-voltage operating block HVB can operate sufficiently. Consequently, when the output
25 voltage V_o has surpassed the first reference voltage V_{ref1} ,

the second driver DR2 starts operating, and the first driver DR1 halts. The comparator CP0 owns a hysteresis characteristic in order to stabilize comparison operation.

The soft start block SSB has a soft start circuit
5 SSC, a soft start capacitor C_{ss} and a soft start activation
switch Q2. The soft start circuit SSC is connected in
series to the external capacitor C_{ss} by way of a soft start
terminal P_{ss}. A node between the soft start terminal P_{ss}
and the external capacitor C_{ss} is connected to the earth by
10 way of the soft start activation switch Q2 serving as an
NMOS transistor. The soft start circuit SSC produces an SS
voltage serving as a DTC voltage. Hence, in order to
produce an SS voltage which is to serve as the DTC voltage,
the soft start circuit SSC is formed from a resistance-type
15 potential divider circuit which divides the power supply
voltage by resistance and outputs the thus-divided voltage.
A high-level or low-level output from the comparator CP0
is applied to a gate of the activation switch Q2.

Operation of the switching power supply unit 200
20 having such a configuration; particularly, operation of the
switching power supply unit 200 performed at start-up, will
be described further by reference to Fig. 4.

When the oscillator OSC1 has started oscillating
operation at point in time t₁, the switching power supply
25 unit 200 starts operation. Immediately after the

oscillator OSC1 has started operation, the output voltage V_o corresponds to the battery voltage V_{bat} , which is lower than the first reference voltage V_{ref1} ($V_o < V_{ref1}$). Hence, an output from the comparator CP0 is at high level.

5 Therefore, the second driver DR2 remains inoperative; the activation switch Q2 remains at on-state; and the first driver DR1 remains in an operating state. Individual circuits of the low-voltage operating block LVB also operate at the battery voltage V_{bat} , which is a low
10 voltage. Hence, the oscillator OSC1 outputs a rectangular wave pulse having a predetermined frequency. The rectangular wave pulse is amplified by the first driver DR1, whereby the amplified pulse is output as a control signal Sout by way of the control signal output terminal
15 Pout1 to control the on-off states of the switching transistor Qo.

As a result of on-off control of the switching transistor Qo, the output voltage V_o gradually increases in the manner shown in Fig. 4, by means of charging and
20 discharging energy into and from the inductor L_o .

At a point in time t_2 at which the output voltage V_o has increased and surpassed the first reference voltage V_{ref1} , the output from the comparator CP0 is inverted to a low level. As a result, the first driver DR1 shifts from
25 an operating state to an inoperative state, whereas the

second driver DR2 shifts from the inoperative state to the operating state. Further, the activation switch Q2 is turned off to start recharging the capacitor C_{ss}. Thus, soft start operation for PWM control is started.

5 The output voltage V_o achieved at the point in time t₂ corresponds to the first reference voltage V_{ref1} at which individual circuits of the high-voltage operating block HVB can operate sufficiently. However, the soft start operation is commenced at the point in time t₂.
10 Hence, the control signal S_{out} is not output until the SS voltage V_{ss} attains a level at which the voltage can be compared with the triangular wave signal CT. Consequently, the capacitor C_o is not recharged with any more electric charge whereby the output voltage V_o cannot increase. This
15 period is indicated by α in the drawing. Subsequently, as the SS voltage V_{ss} increases, PWM control is performed by taking the SS voltage V_{ss} as a reference voltage, whereupon the output voltage V_o increases.

At the point in time t₁ and subsequent points, the
20 feedback voltage V_{fb} is lower than the second reference voltage V_{ref2}, whereby the error output signal E_o remains at a high level continuously. The PWM comparator CP2 compares the triangular wave signal CT with the error output signal E_o or the SS voltage V_{ss}, whichever signal is
25 lower. When the feedback voltage V_{fb} approaches the second

reference voltage V_{ref2} as a result of an increase in the output voltage V_o , the error output signal EO decreases. At a point in time t_3 at which the error output signal EO becomes equal to the ever-increasing SS voltage V_{ss} , the control reference used for PWM control shifts from the SS voltage V_{ss} to the error output signal EO . As a result, normal feedback control is performed, and the output voltage V_o is subjected to PWM control such that the feedback voltage V_{fb} becomes equal to the second reference voltage V_{ref2} .

In the conventional switching power supply unit, when operation of the low-voltage operating block LVB is switched to operation of the high-voltage operating block HVB at time t_2 shown in Fig. 4, there arise a period during which an oscillating operation stops and a period during which only a pulse width narrower than a required pulse width is obtained. Therefore, although it depends on its load conditions, a start-up failure might arise under such a condition that the output voltage V_o is supplied to a load during the period α shown in Fig. 4 and subsequent periods during which a PWM pulse width is narrow, whereby the charge in the capacitor C_o are supplied to the load, and consequently, the output voltage V_o decreases.

If, as a result of a decrease in the output voltage V_o , the output voltage V_o has becomes lower than the first

reference voltage V_{ref1} in excess of the hysteresis width of the comparator CP0, the output of the comparator CP0 again attains a high level, thereby turning on the activation switch Q2. As a result, the capacitor C_{ss} that
5 is being charged might be discharged. The switching operation and the soft start operation are again started after the output voltage V_o has been fully recovered by operation of the low-voltage operating block LVB. When these operations are repeated, an start-up failure might
10 arise.

In order to avoid occurrence of such a situation, if soft start for PWM control is omitted, a large rush current might flow when it is switched from the control operation by the low-voltage operating block LVB to the control
15 operation by the high-voltage operating block HVB. This might bring about adverse effect to the battery power supply or cause an inconvenience of a large drop in the battery voltage V_{bat} .

The control operation by the low-voltage operating
20 block LVB is ON/OFF control without a feedback due to the rectangular pulse of the oscillator OSC1. Hence, there arises a problem that a rush current flows at the time of start-up.

There may also arise a problem that ringing in the
25 output voltage V_o occurs around at the timing of t_3 when

the control reference voltage to be compared with the triangular wave signal CT shifts from the SS voltage Vss to the error output signal EO.

Summary of the Invention

5 The object of the invention is to provide a switching power supply unit having a low-voltage operating block and a high-voltage operating block to produce a higher DC voltage from a low power supply voltage, and a controller IC thereof, which prevents occurrence of a rush current and
10 a start-up failure at switching.

Another object of the invention is to shorten overall start-up time by smooth switching control operation.

The invention provides a switching power supply unit having a switching power supply section for converting an
15 input voltage Vbat into a higher output voltage Vo by switching in accordance with a switching control signal Sout, and to output the higher output voltage Vo; a soft start section SSB-A for producing a soft start voltage Vss which gradually increases at start-up; a voltage comparing
20 comparison section CP0 for comparing the output voltage Vo with a first reference voltage Vref1; a low-voltage circuit section LVB-A, which compares the soft start voltage Vss with a feedback voltage Vfb obtained by feeding back the output voltage Vo, for producing a pulse signal when the

soft start voltage V_{ss} is high; and a high-voltage circuit section HVB-A, which compares either a second reference voltage V_{ref2} or the soft start voltage V_{ss} with the feedback voltage V_{fb} according to a relationship of a level
5 of the second reference voltage V_{ref2} and a level of the soft start voltage V_{ss} to produce an error signal E_O , for producing a PWM control signal based on a comparison result of the error signal E_O with a triangular wave signal CT , wherein when the output voltage V_o is lower than the first
10 reference voltage V_{ref1} , the pulse signal is output as the switching control signal S_{out} , and when the output voltage V_o is higher than the first reference voltage V_{ref1} , the PWM control signal is output as the switching control signal S_{out} .

15 Furthermore, the low-voltage circuit section LVB-A involves a comparator $CP1$ for producing a comparison output when the soft start voltage V_{ss} is higher than the feedback voltage V_{fb} ; a pulse generator $OSC1$ for producing a pulse signal according to the comparison output from the
20 comparator $CP1$; and a first driver $DR1$, which is driven by the comparison output from the voltage comparing section $CP0$, for outputting the pulse signal as the switching control signal S_{out} , and the high-voltage circuit section HVB-A involves an error amplifier E_{amp} , which has either
25 the second reference voltage V_{ref2} or the soft start

voltage V_{ss} with the feedback voltage V_{fb} according to a relationship of level of the second reference voltage V_{ref2} and a level of the soft start voltage V_{ss} to produce the error signal E_O , for feeding back the error signal E_O to
5 the feedback voltage by way of a feedback element; a triangular wave signal oscillator $OSC2$ for producing the triangular wave signal CT ; a PWM comparator $CP2$ for producing the PWM control signal based on a comparison the error signal E_O with the triangular wave signal CT ; and a
10 second driver $DR2$, which is driven by the comparison output from the voltage comparing section $CP0$, for outputting the PWM control signal as the switching control signal S_{out} .

The invention provides a controller IC for controlling a switching power supply section for converting
15 an input voltage V_{bat} into a higher output voltage V_o by switching in accordance with a switching control signal S_{out} , to output the higher output voltage V_o , having a soft start circuit SSC , which cooperates with a capacitor C_{ss} , for producing a soft start voltage V_{ss} which gradually
20 increases at start-up; a voltage comparing section $CP0$ for comparing the output voltage V_o with a first reference voltage V_{ref1} ; a low-voltage circuit section $LVB-A$, which compares the soft start voltage V_{ss} with a feedback voltage V_{fb} obtained by feeding back the output voltage V_o , for
25 producing a pulse signal when the soft start voltage V_{ss} is

high; and a high-voltage circuit section HVB-A, which compares either a second reference voltage V_{ref2} or the soft start voltage V_{ss} with the feedback voltage V_{fb} according to a relationship of a level of the second
5 reference voltage V_{ref2} and a level of the soft start voltage V_{ss} to produce an error signal E_O , for producing a PWM control signal based on a comparison result of the error signal E_O with a triangular wave signal CT , wherein when the output voltage V_o is lower than the first
10 reference voltage V_{ref1} , the pulse signal is output as the switching control signal S_{out} , and when the output voltage V_o is higher than the first reference voltage V_{ref1} , the PWM control signal is output as the switching control signal S_{out} .

15 Furthermore, the low-voltage circuit section LVB-A involves a comparator $CP1$ for producing a comparison output when the soft start voltage V_{ss} is higher than the feedback voltage V_{fb} ; a pulse generator $OSC1$ for producing a pulse signal according to the comparison output from the
20 comparator $CP1$; and a first driver $DR1$, which is driven by the comparison output from the voltage comparing section $CP0$, outputting the pulse signal as the switching control signal S_{out} , and the high-voltage circuit section HVB-A involves an error amplifier E_{amp} , which compares either the
25 second reference voltage V_{ref2} or the soft start voltage

Vss with the feedback voltage Vfb according to a relationship of a level of the second reference voltage Vref2 and a level of the soft start voltage Vss to produce the error signal EO, for feeding back the error signal EO
5 to the feedback voltage by way of a feedback element; a triangular wave signal oscillator OSC2 for producing the triangular wave signal CT; a PWM comparator CP2 for producing the PWM control signal based on a comparison result of the error signal EO with the triangular wave
10 signal CT; and a second driver DR2, which is driven by the comparison output from the voltage comparing section CP0, for outputting the PWM control signal as the switching control signal Sout.

Moreover, the controller IC further has an external
15 terminal Pss to which is connected the capacitor C_{ss} for producing the soft start voltage Vss in cooperation with the soft start circuit SSC.

Brief Description of the Drawings

Fig. 1 is a view showing the configuration of a
20 switching power supply unit according to an embodiment of the invention;

Fig. 2 is a view schematically showing a characteristic achieved at the time of start-up operation of the switching power supply unit shown in Fig. 1;

Fig. 3 is a view showing the configuration of a related-art switching power supply unit; and

Fig. 4 is a view schematically showing a characteristic achieved at the time of start-up operation
5 of the switching power supply unit shown in Fig. 3.

Detailed Description of the Preferred Embodiments

An embodiment of a switching power supply unit according to the invention and a controller IC thereof will be described hereinbelow by reference to the drawings.

10 Fig. 1 is a view showing the configuration of a switching power supply unit according to a first embodiment of the invention. Fig. 2 is a view schematically showing a characteristic of the switching power supply unit at the time of start-up.

15 The switching power supply unit 100 shown in Fig. 1 differs from the conventional switching power supply unit 200 shown in Fig. 3 in terms of a low-voltage operating block LVB-A, a high-voltage operating block HVB-A, and a soft start block SSB-A, which are in a controller IC 10.

20 Other parts of the switching power supply unit 100 are identical with each other of the conventional switching power supply unit 200. Therefore, explanations are primarily given of differences between the switching power supply unit 100 of the invention and the conventional

related-art switching power supply unit 200. In order to avoid redundancy, explanations for same parts are omitted.

The soft start block SSB-A has a soft start circuit SSC and a capacitor C_{ss} . The soft start circuit SSC is
5 connected in series to the external capacitor C_{ss} by way of a soft start terminal P_{ss} . A voltage appearing at a node between the soft start circuit SSC and the external capacitor C_{ss} is an SS voltage V_{ss} . The soft start circuit SSC is formed from, e.g., a constant current source
10 circuit. The soft start circuit SSC starts operation when a start signal ST is applied. The SS voltage V_{ss} is supplied to the low-voltage operating block LVB-A and the high-voltage operating block HVB-A.

The low-voltage operating block LVB-A has a voltage
15 comparator CP1, an oscillator OSC1 and a first driver DR1. In the voltage comparator CP1, the SS voltage V_{ss} is input to a non-inverted input terminal (+), and a feedback voltage V_{fb} is input to an inverted input terminal (-). The voltage comparator CP1 compares these two inputs with
20 each other to produce a high-level output when the SS voltage V_{ss} is higher than the feedback voltage V_{fb} , and the high-level output is applied to the oscillator OSC1.

The oscillator OSC1 performs oscillation while the oscillator OSC1 receives the high-level signal from the
25 voltage comparator CP1. Conversely, the voltage comparator

CP1 suspends oscillation while the voltage comparator CP1 receives a low-level signal. The rectangular wave pulse signal produced by oscillation of the oscillator OSC1 is supplied to the first driver DR1. In other words,
5 according to the invention, the low-voltage operating block LVB-A performs a kind of pulse frequency modulation (PFM). The first driver DR1 is identical with that shown in Fig. 3.

The high-voltage operating block HVB-A has an error
10 amplifier Eamp, a triangular signal oscillator OSC2, a PWM comparator CP2 and a second driver DR2. In the error amplifier Eamp, a second reference voltage Vref2 is input to a first non-inverted input terminal (+), and the feedback voltage Vfb is input to a inverted input terminal
15 (-). In this regard, the error amplifier Eamp is identical with that of being shown in Fig. 3. According to the invention, the error amplifier Eamp further has a second non-inverted input terminal (+) to which the SS voltage Vss is input. An internal circuit of the error amplifier Eamp
20 is configured such that the signal input to the first non-inverted input terminal or the signal input to the second non-inverted input terminal, whichever signal is smaller, is prioritized. Consequently, the SS voltage Vss or the second reference voltage Vref2, whichever voltage is lower,
25 acts as a control reference voltage and is compared with

the feedback voltage V_{fb} . An error output signal EO , which is a result of the comparison, is fed back to the feedback voltage V_{fb} by way of a resistor $R3$ and a capacitor $C1$ and is input to a non-inverted input terminal (+) of the PWM comparator $CP2$.

The triangular oscillator $OSC2$ is identical with that of being shown in Fig. 3, and a triangular wave signal CT oscillated in the triangular oscillator $OSC2$ is input to an inverted input terminal (-) of the PWM comparator $CP2$. The error output signal EO and the triangular wave signal CT are input to the PWM comparator $CP2$. The PWM comparator $CP2$ compares these two signals to produce high-level output only while the error output signal EO is higher than the triangular wave signal CT . That is, the PWM comparator $CP2$ outputs a PWM control signal whose pulse width is controlled according to the magnitude of the error output signal EO . The PWM control signal output from the PWM comparator $CP2$ is supplied to the second driver $DR2$. The second driver $DR2$ is identical with that shown in Fig. 3.

Operation of the switching power supply unit having such a configuration, particularly operation at start-up of the switching power supply unit, will be described further by reference to Fig. 2.

As shown in Fig. 1, the battery voltage V_{bat} is supplied to the controller IC 10, which produces a state of

the output voltage V_o being zero, so that the start signal ST is supplied to the soft start circuit SSC at the time t_1 . As a result, the switching power supply unit 100 starts up. When the start signal ST is supplied, a
5 constant current flows from the constant current circuit of the soft start circuit SSC to the capacitor C_{ss} so as to enable the charged voltage of the capacitor C_{ss} or the SS voltage V_{ss} to rise gradually.

The SS voltage V_{ss} is supplied to both the voltage
10 comparator CP1 and the error amplifier Eamp. The feedback voltage V_{fb} is also supplied to both the voltage comparator CP1 and the error amplifier Eamp. During start-up period, the SS voltage V_{ss} is lower than the second reference voltage V_{ref2} . Therefore, the SS voltage V_{ss} is compared
15 with the feedback voltage V_{fb} by means of the voltage comparator CP1 and the error amplifier Eamp.

In the high-voltage operating block HVB-A, even when the power supply voltage utilizing the output voltage V_o is low, the error amplifier Eamp, the oscillator OSC2 and the
20 PWM comparator CP2 attempt to operate respectively. However, while the power supply voltage is low, operation reliability of these devices is low. Therefore, the PWM control signal output from the PWM comparator CP2 is blocked by the second driver DR2. As the operation
25 reliability of these devices increases with an increase of

the power supply voltage, the PWM control signal is utilized when the devices have become sufficiently reliable.

In the low-voltage operating block LVB-A, the first
5 driver DR1 operates. The voltage comparator CP1 outputs a high-level voltage when the SS voltage V_{ss} is higher than the feedback voltage V_{fb} . As a result, the oscillator OSC1 oscillates to produce a pulse signal. The pulse output is supplied to the switching transistor Q_o as a switching
10 control signal S_{out} by way of the first driver DR1 in operation. By means of on/off operation of the switching transistor Q_o , the output voltage V_o increases gradually.

When the feedback voltage V_{fb} has become higher than the SS voltage V_{ss} as a result of that the output voltage
15 V_o increased, the voltage comparator CP1 outputs a low-level voltage, and the oscillator OSC1 stops oscillation. For this reason, the output voltage V_o increases with an increase of the SS voltage V_{ss} .

During start-up period, the low-voltage operating
20 block LVB-A is subjected to soft start control in accordance with the SS voltage V_{ss} . Hence, the switching power supply unit can be started up smoothly without flow of a rush current.

Once the output voltage V_o has reached the first
25 reference voltage V_{ref1} at the time t_2 , the output of the

comparator CP0 is inverted, that is, the output of the comparator CP0 drops from a high level to a low level. As a result, the first driver DR1 becomes inoperative, and the second driver DR2 becomes operative. The first reference
5 voltage Vref1 is set to a voltage at which operation of the high-voltage operating block HVB-A is sufficiently reliable.

The error amplifier Eamp, the triangular wave oscillator OSC2 and the PWM comparator CP2 operate
10 according to the relation of the SS voltage Vss and the feedback voltage Vfb before the second driver DR2 has become operative, to thus produce the PWM control signal. At the time t2 when the second driver DR2 becomes operative, the reliability of the PWM control signal has
15 become sufficiently high.

At the time t2, the control signal Sout is switched from the pulse signal of the low-voltage operating block LVB-A to the PWM control signal of the high-voltage operating block HVB-A.

20 Both the pulse signal of the low-voltage operating block LVB-A and the PWM control signal of the high-voltage operating block HVB-A are based on the SS voltage Vss and the feedback voltage Vfb. Hence, shock stemming from switching operation becomes very small. A shock might be
25 determined by means of only a difference between the degree

of accuracy of the control performed through on/off operation of oscillating operation and the degree of accuracy of the PWM control or a difference between the degrees of elaboration of the control operations.

5 Consequently, the switching operation can be performed smoothly.

Even after the control has been switched to the PWM control at the time t_2 , the SS voltage V_{ss} continues increasing, and the output voltage V_o increases
10 correspondingly.

The soft start control operation is completed when the SS voltage V_{ss} has reached the second reference voltage V_{ref2} at time t_3 . At the time t_3 , a voltage for comparing with the error amplifier E_{amp} shifts from the SS voltage
15 V_{ss} to the second reference voltage V_{ref2} . From the time t_3 onward, the PWM control is performed so that the feedback voltage V_{fb} becomes equal to the second reference voltage V_{ref2} . When the reference voltage for comparison shifts from the SS voltage V_{ss} to the second reference
20 voltage V_{ref2} , ringing such as the conventional does not occur to the output voltage V_o .

As mentioned above, during the period T_1 from the starting time t_1 to the switching time t_2 , the PFM control is performed by the low-voltage operating block LVB-A.
25 During a period T_2 from the switching time t_2 to the time

t3 (the time when the soft start control operation completes), the PWM control operation on the basis of the SS voltage Vss is performed by the high-voltage operating block HVB-A. During an ordinary operation period T3 after
5 the time t3, the PWM control operation on the basis of the second reference voltage Vref2 is performed by the high-voltage operating block HVB-A.

According to the invention, the switching power supply unit can smoothly start operation by means of the
10 PFM control performed by the low-voltage operating block LVB-A even at the starting time t1. Even at the switching time t2, switching can be made smoothly from the PFM control operation performed by the low-voltage operating block LVB-A to the PWM control operation performed by the
15 high-voltage operating block HVB-A. As the control operation is smoothly switched at the time t2, a required time (T1+T2) for start-up operation can be more shortened than the conventional.

The voltage comparator CP1 and the oscillator OSC1 as
20 well as the first driver DR1, that is, the entire low-voltage operating block LVB-A, may be made inoperative by means of an output from the comparator CP0. In this case, there can be diminished the power dissipated by the low-voltage operating block LVB-A which is not used during an
25 ordinary operation performed after start-up.

The capacitor C_{ss} may be not outside but inside the controller IC₁₀. In this case, the soft start terminal P_{ss} may be omitted.

5 The resistors R₁, R₂, R₃ and the capacitor C₁ may be provided not outside but inside the controller IC₁₀. In this case, the feedback voltage terminal P_{fb} and the error output terminal P_{eo} can be omitted by utilization of the output voltage terminal P_{vo}.

10 According to the embodiment, the switching power supply unit 100 has the low-voltage operating block LVB-A and the high-voltage operating block HVB-A as control sections for the purpose of producing a higher DC voltage from a low power supply voltage and a controller IC thereof, the low-voltage operating block LVB-A and the
15 high-voltage operating block HVB-A are controlled on the basis of the same soft start voltage at start-up. At the time an output DC voltage has reached an expected value, it is switched from a control signal of the low-voltage operating block LVB-A to a control signal of the high-
20 voltage operating block HVB-A. Basically, a variation does not arise in the output voltage between before and after switching operation. Hence, switching is performed smoothly.

The high-voltage operating block HVB-A effectively
25 performs control immediately after the control performed by

the low-voltage operating block LVB-A has been switched to the control performed by the high-voltage operating block HVB-A. Hence, the risk of occurrence of a start-up failure, which would otherwise could be caused by the conventional switching power supply unit, can be
5 eliminated.

When the control performed by the low-voltage operating block LVB-A is switched to the control performed by the high-voltage operating block LVB-A, there is no time
10 at which voltage control is halted, which would otherwise arise in the conventional. Hence, the required time to boost a voltage to a predetermined DC voltage can be shortened.